PATENT

REMARKS

Claims 1-23 remain pending in the application. Claims 1, 13, and 20 have been amended. For the convenience and reference of the Examiner all currently pending claims, including those unchanged by this amendment, are reproduced in the Version Showing Changes Made attached hereto.

Embodiments of methods in accordance with the present invention relate to deposition of material into gaps or recesses formed between adjacent raised surfaces on a semiconductor workpiece, such that voids are not formed in the features. As discussed in connection with Figure 3 reproduced below, particular embodiments of the invention address formation of voids attributable to reentrant cavities present in recess sidewalls:

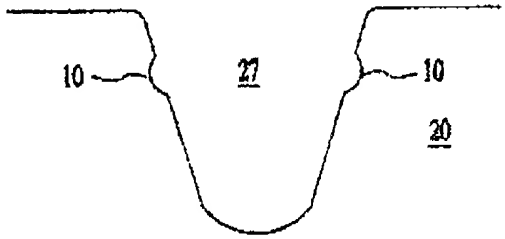

FIG. 3
(PRIOR ART)

> [0010] Generally, the recesses 27 which are not easily filled without forming voids 30 are those which have non-smooth profiles with some reentrant cavities 10 thereon, as shown in Figure 3. To find a method for filling these recesses 27, precursor gas compositions having different O_3 concentrations, and different process temperatures were tried. Although using different process parameters was determined to improve recess filling a little, the voids 30 were still formed in some of the recesses 27 because of their non smooth profiles. For example, voids 30 were formed even in the small tapered recesses 27 when the sidewalls of the tapered recesses 27 had the reentrant cavities 10. (Emphasis added)

In an effort to prevent formation of voids attributable to such reentrant side wall cavities, the present inventors have devised a method for depositing material from the

bottom of the feature upward, which exploits differing rates of deposition over various portions of the recess. This aspect may be better understood with reference to Figure 4B and explanatory text:

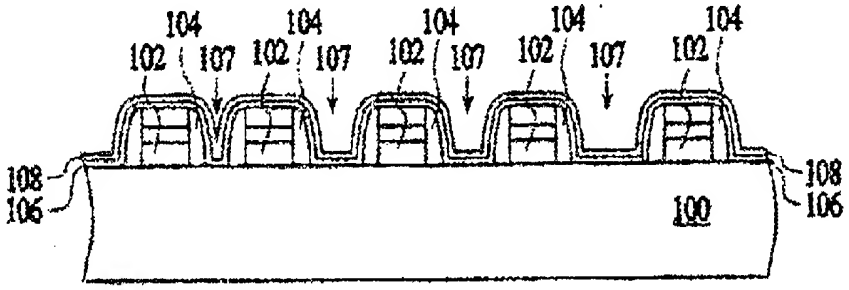

FIG. 4B

[0017] Referring to Figure 4B, in a first stage, a first layer 108 is deposited in the recesses 27 and over the substrate 100. In this stage, a deposition gas composition that provides different deposition rates depending upon the underlying material upon which the deposition occurs, is used. In one version, the deposition gas comprises an oxygen-containing compound, such as one or more of O_3 or TEOS. A suitable deposition gas composition comprises first and second components such as O_3 and TEOS, in a volumetric flow ratio that provides different deposition rates on silicon or silicon oxide material. (Emphasis added)

Thus while the simplified view of Figs. 4B shows silicon nitride liner 106 covering both recess sidewalls and bottoms, the composition of the material underlying nitride liner 106 in fact influences the rate of oxide deposition. This effect of the underlying substrate is explained in detail in the following articles, now submitted in a supplemental information disclosure statement: Kwok et al., "Surface Related Phenomena in Integrated PECVD/Ozone-TEOS SACVD Processes for Sub-Half Micron Gap Fill: Electrostatic Effects", J. Electrochem. Soc. Vol. 141, No. 8 (1994), and Fujino et al., "Dependence of Deposition Characteristics on Base Materials in TEOS and Ozone CVD at Atmospheric Pressure", J. Electrochem. Soc. Vol. 138, No. 2 (1991). In

particular, these references indicate that under certain processing conditions, oxide may be deposited more rapidly on silicon surfaces than on oxide surfaces.

Embodiments in accordance with the present invention exploit this property to achieve uniform gap fill without the presence of voids. Referring again to Figure 4B of the instant application, oxide deposition occurs more rapidly on the nitride liner overlying silicon at the bottom of the recess, and occurs less rapidly on the nitride liner overlying non-silicon on the recess side walls. This combination of deposition rates results in desired filling of the recess from the bottom upward, without formation of voids due to reentrant cavities.

In the office action mailed July 25, 2002, the Examiner rejected each of pending claims 1-23, either as anticipated by U.S. patent no. 6,331,494 to Shufflebotham et al. ("the Shufflebotham patent") or as obvious under the Shufflebotham patent considered in light of U.S. patent no. 6,331,494 to Olsen et al. ("the Olsen patent").

The Shufflebotham patent is entitled "Method of High Density Plasma CVD Gap-Filling" (Emphasis added). The Shufflebotham patent describes a process for forming oxide over features of a semiconductor device, emphasizing that the high density plasma chemical vapor deposition (HDP-CVD) of oxide suppresses formation of voids in filled features through sputtering of material deposited on feature side walls:

> RF power applied to the chuck, which produces a net negative DC bias on the wafer surface, accelerates positive ions onto the wafer surface, which sputters the growing film. . . . For normally incident ions, sputtering will be most pronounced on the top corners of the lines, and will form 45° facets. Thus, the very features that would tend to close off the top of a gap during deposition are exactly those features which are sputtered most rapidly. Control over the ion dynamics is critical in the gap-fill process. (Emphasis added; col. 6, lines 52 - 66).

The Olsen patent relied upon by the Examiner similarly describes formation of silicon oxide within features of a semiconductor device, again emphasizing that void formation is suppressed by the combined action of deposition and sputtering attributable to high density plasma:

> A key feature of an inventive method is that deposition and sputtering of the carbon-containing low dielectric constant silicon oxide material ("the material") may occur simultaneously at the wafer substrate. The sputtering of the material occurs as a result of the high F rf bias applied to the substrate holder. Gas molecules that have been ionized in the high density plasma, particularly argon, accelerate toward the wafer substrate surface when the bias is applied to the substrate. Material is thereby sputter etched when the ions strike the surface. As a result, the material is sputter etched to help keep gaps open during the deposition process. (Emphasis added; col. 10, lines 29 - 40)

In contrast with the HDP-CVD approaches described by both the Shufflebotham and Olsen patents, the instant application does not rely upon or even mention the sputtering action of ions in a high density plasma to ensure gap fill without void formation. Rather, as emphasized above, embodiments in accordance with the present invention suppress void formation by exploiting differences in the rate of deposition of oxide material over various surfaces.

To highlight this aspect of the invention, independent claim 1 has now been amended to recite differential rates of deposition of the first layer of material on the side walls and bottom of the recess:

> 1. (Amended) A deposition method capable of filling recesses in a substrate, the method comprising:
>
> (a) providing a substrate having recesses defining side walls and recess bottoms;
>
> (b) exposing the substrate to an energized deposition gas comprising first and second components, to deposit a first layer of a material in the recess at different rates over the side walls and recess bottoms; and
>
> (c) reducing the ratio of the first component to the second component, to deposit a second layer of the material over the first layer in the recess.

Independent claims 13 and 20 have been amended in a manner similar to claim 1.

Deposition without sputtering in accordance with the claimed methods of the present invention poses a number of benefits relative to HDP-CVD processes taught by the Shufflebotham and Olsen patents. One potentially important advantage is that

deposition need not take place in the presence of a high density plasma giving rise to sputtering. In some embodiments of the present invention, reaction between gases to form the deposited material may result from excitation by a lower density plasma that does not result in sputtering. Such non-high density plasma processes are cost effective relative to HDP-CVD processes, which require more complex machinery and exhibit greater performance sensitivity to variation in process parameters. In addition, such non-high density plasma deposition approaches may avoid damaging by sputtering, the fragile semiconducting structures present on the wafer.

Moreover, alternative embodiments in accordance with the present invention may utilize mechanisms other than plasma formation to excite reactant gases and cause deposition of material. For example, sub-atmospheric chemical vapor deposition (SACVD) processes utilize reduced ambient pressure to perform deposition. Again, such alternative approaches may prove significantly more cost-effective than HDP-CVD, especially considering the expense and effort required to create and sustain a uniform high density plasma within a processing chamber during deposition.

In view of the foregoing amendments and remarks, Applicants believe that all claims pending in this application are now in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

Kent J. Tobin
Reg. No. 39,496

TOWNSEND and TOWNSEND and CREW LLP
Tel: (650) 326-2400
Fax: (650) 326-2422
KJT:km
PA 3246200 v1 xxx

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 1, 13 and 20 have been amended in the manner shown below:

1. (Amended) A deposition method capable of filling recesses in a substrate, the method comprising:

(a) providing a substrate having recesses defining side walls and recess bottoms;

(b) exposing the substrate to an energized deposition gas comprising first and second components, to deposit a first layer of a material in the recess at different rates over the side walls and recess bottoms; and

(c) reducing the ratio of the first component to the second component, to deposit a second layer of the material over the first layer in the recess.

13. (Amended) A deposition method capable of filling recesses in a substrate, the method comprising:

(a) providing a substrate having recesses defining side walls and recess bottoms;

(b) exposing the substrate to an energized deposition gas comprising a first volumetric flow ratio of O_3 and TEOS, to deposit a first layer of silicon oxide in the recess at different rates over the side walls and recess bottoms; and

(c) reducing the volumetric flow ratio of the O_3 to the TEOS, to deposit a second layer of silicon oxide over the first layer in the recess.

20. (Amended) A deposition method capable of filling recesses on a substrate, the recesses being between polysilicon gates and having sidewall portions covered with silicon nitride spacers, and wherein the silicon nitride spacers, the polysilicon gates and the other portions of the substrate, are covered with a silicon nitride liner, the method comprising:

(a) providing an energized deposition gas comprising O_3 and TEOS, to form a first layer of silicon oxide in the recess at different rates over side walls and recess bottoms of the recess; and

(b) reducing the volumetric flow ratio of O_3 to TEOS in the deposition gas, to fill the recesses with silicon oxide after the first layer is formed.

Claims 2-12, 14-19, and 21 remain unchanged by this amendment.

2. (Unchanged) A method according to claim 1 wherein one or more of the first and second components comprise oxygen-containing compounds.

3. (Unchanged) A method according to claim 1 wherein the first component comprises O_3.

4. (Unchanged) A method according to claim 3 wherein the ratio-reducing step is performed by reducing the flow rate of O_3.

5. (Unchanged) A method according to claim 4 wherein the ratio-reducing step is performed for about 30 seconds.

6. (Unchanged) A method according to claim 3 wherein the second component comprises TEOS.

7. (Unchanged) A method according to claim 1 wherein the ratio-reducing step comprises reducing a flow rate of the first component.

8. (Unchanged) A method according to claim 7 wherein the flow rate of the first component is gradually reduced.

9. (Unchanged) A method according to claim 8 wherein the ratio-reducing step is performed for about 30 seconds.

10. (Unchanged) A method according to claim 1 comprising providing a substrate having recesses between polysilicon gates.

11. (Unchanged) A method according to claim 10 wherein the recesses have sidewall portions covered with silicon nitride spacers, and wherein the silicon nitride spacers, the polysilicon gates and the other portions of the substrate, are covered with a silicon nitride liner.

12. (Unchanged) A method according to claim 1 wherein the first layer has a thickness of from about 200 to about 800 angstroms.

14. (Unchanged) A method according to claim 13 wherein the ratio-reducing step comprises reducing a flow rate of the O_3.

15. (Unchanged) A method according to claim 13 wherein the ratio-reducing step is performed for about 30 seconds.

16. (Unchanged) A method according to claim 13 wherein the recesses are between polysilicon gates and have sidewall portions covered with silicon nitride spacers, and wherein the silicon nitride spacers, the polysilicon gates and the other portions of the substrate, are covered with a silicon nitride liner.

17. (Unchanged) A method according to claim 16 wherein the silicon nitride liner comprises reentrant cavities, and wherein the reentrant cavities are smoothened by the first layer.

18. (Unchanged) A method according to claim 13 comprising depositing the first layer to a sufficient thickness to fill the reentrant cavities.

19. (Unchanged) A method according to claim 18 comprising depositing the first layer to a thickness of from about 200 to about 800 angstroms.

21. (Unchanged) A method according to claim 20 wherein the ratio-reducing step is performed by reducing the flow rate of O_3.

22. (Unchanged) A method according to claim 20 wherein the ratio-reducing step is performed for about 30 seconds.

23. (Unchanged) A method according to claim 20 comprising depositing the first layer to a thickness of from about 200 to about 800 angstroms.